AMENDMENTS TO THE SPECIFICATION

Please replace the section titled "In the Brief Description of the Drawings" on page 12, beginning at line 16, through page 21 with the following amended paragraph. This section also incorporates the amendments from the Preliminary Amendment submitted with the original filing of the application:

Brief Description of the Drawings

A better understanding of the present invention can be obtained when the following detailed description of the preferred embodiment is considered in conjunction with the following drawings, in which:

Fig. 1 is a schematic architectural overview of the basic modules of the circuit C;

Fig. 2 is a schematic illustration of the physical layout of circuit C;

Fig. 3 (comprising Figs. 3A and 3B) is a table summarizing pin assignments for the circuit C;

Fig. 4 (comprising Figs. 4A and 4B) is an alternative layout diagram for the ~~circuit C;~~ circuit C noise and a primary clock signal employed by the circuit C;

Fig. 5 is a table summarizing pin assignments for the circuit C grouped by module;

Fig. 6 (comprising Figs. 6A and 6B) is a schematic illustration of a typical full-featured implementation of a PC audio circuit C with associated circuits, buses and interconnections;

Fig. 7 (comprising Figs. 7A and 7B) is table summarizing pin assignments and functions that relate to local memory control;

~~Figs. 8~~ Fig. 8 (comprising Figs. 8A, 8B and 8C), Fig. 9 (comprising Figs. 9A, 9B and 9C) and Fig. 10 (comprising Figs. 10A, 10B and 10C) comprise a table of register mnemonics with indexes and module assignments where appropriate;

Fig. 11 is a schematic diagram illustrating an example of multiplexing circuitry;

Fig. 12 is a block diagram schematic illustration of the system control module of the circuit C;

Fig. 13 is a schematic block diagram of the circuit C including modular interfaces to the register data bus;

Fig. 14a is a schematic diagram of implementation detailed for the register data bus;

Fig. 14b is a schematic diagram of a portion of the ISA bus interface circuitry;

Fig. 15 is a timing diagram illustrating worse case ISA-bus timing for the circuit C;

Fig. 16a is a timing diagram relating to buffered input and outputs for the circuit C;

Fig. 16b is a schematic diagram of a portion of the emulation logic for the circuit C;

Fig. 16c is a schematic block diagram of circuit access possibilities for application software and emulation TSR programs;

Fig. 17 is a schematic illustration of the Plug-n-Play state machine included within the circuit C;

Fig. 18 is a timing diagram relating to reading serial EEPROM data from external circuitry relating to Plug-n- Play compatibility;

Fig. 19 is a schematic illustration of a circuit for facilitating PNP data transfer from external circuitry to the circuit C via the register data bus;

Fig. 20 is a schematic illustration of a linear feed back shift register necessary to implement an initiation key for access to Plug-n-Play registers;

Fig. 21 is a flow chart illustrating the manner in which the Plug-n-Play circuitry associated with the circuit C transitions from isolation mode to either configuration mode or sleep mode;

Fig. 22 is a table summarizing resources required for programming the Plug-n-Play serial EEPROM;

Fig. 23 (comprising Figs. 23A and 23B) is a table providing data on all interrupt-causing events in the circuit C;

Fig. 24a is a schematic illustration of external oscillators and stabilizing logic associated therewith utilized by the circuit C;

Fig. 24b (comprising Figs. 24B-1 and 24B-2) is a schematic illustration of logic and counter circuits associated with various low power modes of the circuit C;

Fig. 24c (comprising Figs. 24C-1 and 24C-2) is a flow chart illustrating the response of circuit C to suspend mode operation;

Fig. 24d (comprising Figs. 24D-1, 24D-2, 24D-3 and 24D-4) is a flow chart illustrating the various register-controlled low power modes of the circuit C;

Fig. 25 is a schematic illustration of details of the clock oscillator stabilization logic of Fig. 24a;

Fig. 26 (comprising Figs. 26A and 26B) is a table describing events which occur in

response to various power conservation modes enabled via the status of bits in register PPWRI contained within the circuit C;

Fig. 27 is a timing diagram showing the relationship between various power conservation modes and signals and clock signals utilized by the circuit C;

Fig. 28 (comprising Figs. 28A, 28B and 28C) is a table summarizing pins associated with the system bus interface included in the circuit C;

Fig. 29 is a block diagram schematically illustrating the basic modules which comprise the local memory control module of the circuit C;

Fig. 30 is a block diagram schematically illustrating the master state machine associated with the local memory control module of the circuit C;

Fig. 31 is a timing diagram illustrating the relationship of suspend mode control signals and a 32 KHz clock signal utilized by the circuit C;

Fig. 32 is a state diagram schematically illustrating refresh cycles utilized by the circuit C during suspend mode operation;

Fig. 33 is a timing diagram for suspend mode refresh cycles;

Fig. 34a is a timing diagram for 8-bit DRAM accesses;

Fig. 34b is a timing diagram for 16-bit DRAM accesses;

Fig. 34c is a timing diagram for DRAM refresh cycles;

Fig. 35 is a timing diagram illustrating how real addresses are provided from the circuit C to external memory devices;

Fig. 36 is a schematic block diagram of a control circuit for local memory record and playback FIFOs;

Fig. 37 is a diagram illustrating the relationship between data stored in system memory and interleaved in local memory via the circuit C;

Fig. 38 is a table describing data transfer formats for 8 and 16-bit sample sizes under DMA control;

Fig. 39 (comprising Figs. 39A and 39B) is a schematic block diagram illustrating circuitry for implementing interleaved DMA data from system memory to local memory via the local memory control module of the circuit C;

Fig. 40 is a schematic block illustration of the game port interface between external devices and the circuit C;

Fig. 41a is a schematic block illustration of a single bit implementation for the game input/output port of the circuit C;

Fig. 41b is a diagram illustrating input signal detection via the game port of the circuit C;

Fig. 42 is a schematic block diagram illustrating the MIDI transmit and receive ports for the circuit C;

Fig. 43 is a timing diagram illustrating the MIDI data format utilized by the circuit C;

Fig. 44 is a block diagram of the various functional blocks of the CODEC module of the present invention;

~~Fig. 45~~ Fig. 45A is a schematic of the preferred embodiment of the left channel stereo mixer of the present invention;

Fig. 45b (comprising Figs. 45B-1 and 45B-2) is a table of gain and attenuation values.

Fig. 46 is a diagram of a partial wave form indicating signal discontinuities for attenuation/gain changes;

Fig. 47 is a block diagram showing zero detect circuits for eliminating "zipper" noise;

Fig. 48 is a block diagram showing clock generation functions in the present invention;

Fig. 49a is a block diagram of serial data transfer functions of the present invention;

Fig. 49b is a block diagram of the serial transfer control block;

Fig. 50 is a block diagram showing internal and external data paths and interfacing with external devices, supported by the present invention;

Fig. 51 is a block diagram of the digital to analog converter block of the present invention;

Fig. 52 is a block diagram of the front end of the digital to analog converter block of the present invention;

~~Fig. 53a-53f~~ Figs. 53A-53F are graphs showing outputs of various stages of the DAC block, including frequency response;

Fig. 54 shows six graphs representing outputs and frequency response of various stages of the DAC block;

Fig. 55 is a schematic representation of the Interp.1 block, phase 1 of Fig. 52;

Fig. 56 is a schematic representation of the Interp.1 block, phase 2 of Fig. 52;

Fig. 57 is a schematic representation of the Interp.2 block of Fig. 52;

Fig. 58 is a graph of the frequency response of the Interp.2 block of Fig. 52;

Fig. 59 is a graph representing the in-band rolloff of the Interp.2 block of Fig. 52;

Fig. 60 is a schematic representation of an embodiment of the Interp.3 block of Fig. 52;

Fig. 61 is a schematic representation of another embodiment of the Interp.3 block of Fig. 52;

Fig. 62a is a graph of the frequency response of the Interp.3 block of Fig. 52;

Fig. 62b is a graph of the passband rolloff of the Interp.3 block of Fig. 52;

Fig. 63 (comprising Figs. 63A and 63B) is a schematic representation of the noise shaper block of Fig. 52;

Fig. 64 is a signal flow graph (SFG) of the noise shaper block in Fig. 52;

Fig. 65 is a plot of the poles and zeros in the *s* plane for the noise shaper block of Fig. 52;

Fig. 66 is a plot of the transfer function magnitude of the noise shaper block of Fig. 52;

Fig. 67 is a plot of the poles and zeros in the *z* plane of the noise shaper block of Fig. 52;

Fig. 68 is a graph of the transfer function of the noise shaper filter of Fig. 52;

Fig. 69 is a plot of the ideal and realizable zeros of the noise filter block of Fig. 52;

Fig. 70 is a plot comparing two embodiments of noise transfer functions for the noise shaper block of Fig. 52;

Fig. 71 is a plot of the noise and signal transfer functions of the noise shaper block of Fig. 52;

Fig. 72 is a plot of the signal transfer function magnitude in phase and passband of the noise shaper block of Fig. 52;

Fig. 73 is a graph of the group delay (sec.) of the noise shaper block of Fig. 52;

Fig. 74 is a graph of the constant attenuation/gain contours of various embodiments of the noise shaper block of Fig. 52;

Fig. 75 plots A_{max} versus noise gain k for an embodiment of the noise shaper block of Fig. 52;

Fig. 76 is a graph of an embodiment of the noise gain k versus band width for g=-90dB of the noise shaper block of Fig. 52.

Fig. 77 is a graph showing the impulse response of the D/A FIR filter;

Fig. 78 is a graph showing the frequency response of the D/A FIR filter;

Fig. 79 schematically illustrates one embodiment of the D/A conversion circuit of the present invention;

Figs. 80 and 81 schematically illustrate another embodiment showing the differential D/A conversion circuit of the present invention;

Fig. 82 is a block diagram of the CODEC ADC of the present invention;

Fig. 83 is a block diagram of the front end of the CODEC ADC;

Fig. 84 is a graph illustrating the sigma-delta modulator output spectrum-range and phase for the ADC of the present invention;

Fig. 85 is a graph illustrating the sigma-delta modulator output spectrum, in detail;

Fig. 86 is a graph illustrating the output spectrum of the sinc6 Decim.1 filter output;

Fig. 87 is a graph illustrating the output spectrum of the half-band Decim.2 filter output;

Fig. 88 is a graph illustrating the output spectrum of the 16-bit Decim.3 filter output;

Fig. 89 is a block diagram of the Decim.1 filter;

Fig. 90 graphically illustrates the frequency response of the Decim.1 filter;

Fig. 91 graphically illustrates a detailed frequency response of the Decim.1 filter;

Fig. 92 is a block diagram of the half-band Decim.2 filter-direct form;

Fig. 93 is a block diagram of the half-band Decim.2 filter-transposed form;

Fig. 94 graphically illustrates the frequency response of the Decim.2 filter;

Fig. 95 is a detailed frequency response graph of the Decim.2 filter;

Fig. 96 is a block diagram of the compensation filter of the CODEC D/A conversion circuitry;

Fig. 97 graphically illustrates the frequency response of the Decim.3 filter;

Fig. 98 graphically illustrates, in detail, the frequency response of the Decim.3 filter;

Fig. 99 graphically illustrates the compensator circuit frequency response (un-compensated);

Fig. 100 graphically illustrates the total frequency response of the compensator circuitry in passband (un-compensated); and

Fig. 101 graphically illustrates the total frequency response of the compensator in passband (compensated).

Fig. 102 is a block diagram of the synthesizer module of the present invention;

Fig. 103 illustrates signal flow in the synthesizer module of the present invention;

Figs. 104a-104f are graphs illustrating addressing control options in the synthesizer module of the present invention;

Figs. 105a-105e are graphs illustrating volume control options in the synthesizer module of the present invention;

Figs. 106a and 106b are graphs of low frequency oscillator waveforms available for the synthesizer module of the present invention;

Fig. 107 (comprising Figs. 107A, 107B and 107C) is an architectural diagram of an address controller of the synthesizer module of the present invention;

Fig. 108a (comprising Figs. 108A-1 and 108A-2) and Fig. 108b (comprising Figs. 108B-1, 108B-2 and 108B-3) are timing diagrams of the operations performed by the address controller of Fig. 107;

Fig. 109 (comprising Figs. 109A, 109B and 109C) is an architectural diagram of a volume controller of the synthesizer module of the present invention;

Fig. 110 (comprising Figs. 110A and 110B) is a timing diagram of the operations performed by the volume controller of Fig. 109;

Fig. 111 is an architectural drawing of the register array of the synthesizer module of the present invention;

Fig. 112 is a timing chart of the operations of the register array in Fig. 111;

Fig. 113 is an architectural drawing of the overall volume control circuitry of the synthesizer module of the preset invention;

Fig. 114a (comprising Figs. 114A-1 and 114A-2) is a logic diagram of a comparator illustrated in Fig. 113;

Fig. 114b is a timing chart of the operations of the comparator in Fig. 114a;

Fig. 115 is an architectural drawing of the LFO generator of the synthesizer module of the present invention;

Fig. 116 (comprising Figs. 116A and 116B) is an architectural diagram of the signal path of the synthesizer module of the present invention;

Fig. 117 (comprising Figs. 117A, 117B, 117C and 117D) is a timing diagram of the operations performed by the signal path of Fig. 116;

Fig. 118 is an architectural diagram of accumulation logic of the synthesizer module of the present invention;

Fig. 119 is a timing diagram of the operations performed by the accumulation logic of Fig. 118;

Fig. 120 (comprising Figs. 120A, 120B, 120C and 120D) is a timing diagram of the overall operations performed by the synthesizer module of the present invention;

Fig. 121 is an amplitude versus time graph illustrating data interpolation; and

Fig. 122 is an amplitude versus time graph illustrating the envelope segments of a musical note.